Notice of Allowability	Application No.	Applicant(s)	
	10/769,591	KULKARNI ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *08/04/06*.

2. ☒ The allowed claim(s) is/are *1-5,7,17-20 and 22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *09/01/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JACK CHIANG
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Keith Chanroon (Reg. No. 36480) on 09/01/06.

The application has been amended as follow:

Claim 1 line 7, after "component" insertion --, to store messages--.

Claim 1 line 9, after "system" insertion --, said memory component is defined by a memory architecture and a memory interface, and said memory-interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface--.

Claim 1 line 14, after "component" insertion --, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories--.

Claim 6 has been canceled.

Claim 7 line 1, change "claim 6" to --claim 1--.

Claim 8 has been canceled.

Claims 9-16 have been canceled.

Claim 17 line 8, after "component" insertion --, to store messages--.

Claim 17 line 10, after "system" insertion --, said memory component is defined by a memory architecture and a memory interface, and said memory-interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface--.

Claim 17 line 15, after "component" insertion --, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories--.

Claim 21 has been canceled.

Claim 22 line 1, change "claim 21" to --claim 17--.

Claim 23 has been canceled.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

Claims 1-5, 7, 17-20, and 22 are allowed because the prior art does not teach or suggest a method of designing a memory system for implementation using an integrated circuit, comprising: configuring a memory component to store messages and a memory interconnection component of a memory model in response to the specification data to generate a logical view of said memory system, said memory component is defined by a memory architecture and a memory interface, and said memory-interconnection component is defined by a memory-interconnection architecture and a memory-interconnection interface; and generating a physical description of said memory system in response to said logical view, said physical description including memory circuitry associated with said integrated circuit defined by said memory component, said memory circuitry having an interconnection topology defined by said memory interconnection component, wherein said memory circuitry comprises a plurality of memories, and wherein said memory architecture is configured to store said messages within said plurality of memories with the combination of all other features corresponding to the independent claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tat Binh
Patent Examiner
September 1, 2006

JACK CHIANG
SUPERVISORY PATENT EXAMINER